

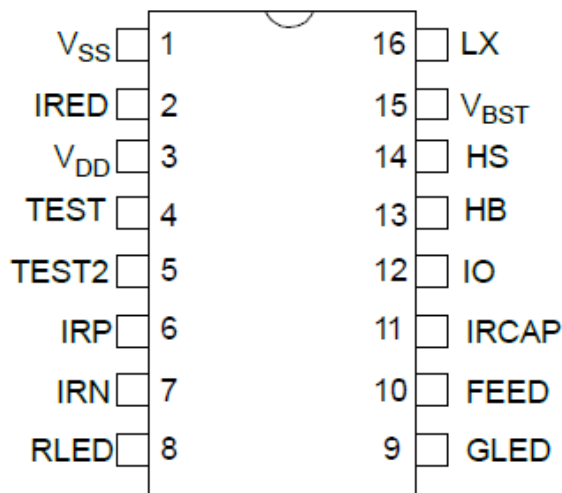
Low Voltage Photoelectric Smoke Detector ASIC with Interconnect and Timer Mode

1.0. INTRODUCTION

1.1 Features

- Low Quiescent Current Consumption
- Two AA Battery Operation
- Internal Power On Reset
- Local Alarm Memory
- Internal Low Battery detector
- Interconnect up to 40 Detectors
- 9 minute Timer for Sensitivity Control
- Temporal or Continuous Horn Pattern
- Low Battery and Chamber Test
- Internal Infrared Emitter Diode (IRED) driver
- Adjustable IRED Drive current
- Adjustable Hush Sensitivity
- Available in SOP16

1.2 Pin Diagrams



1.3 Description

The BL5980 is a low power, low voltage photoelectric type smoke detector IC. With minimal external components, this circuit will provide all the required features for a photoelectric-type smoke detector.

A check for a low battery condition is performed every 86 seconds, and chamber integrity is tested once every 43 seconds, when in Standby. The temporal horn pattern supports the NFPA 72 emergency evacuation signal.

The BL5980 incorporates a gain-selectable photo amplifier for use with an infrared emitter/detector pair.

An internal oscillator strobes power to the smoke detection circuitry every 10 seconds, to keep the standby current to a minimum. If smoke is sensed, the detection rate is increased to verify an Alarm condition. A high gain mode is available for push button chamber testing.

An internal 9 minute timer can be used for a Reduced Sensitivity mode.

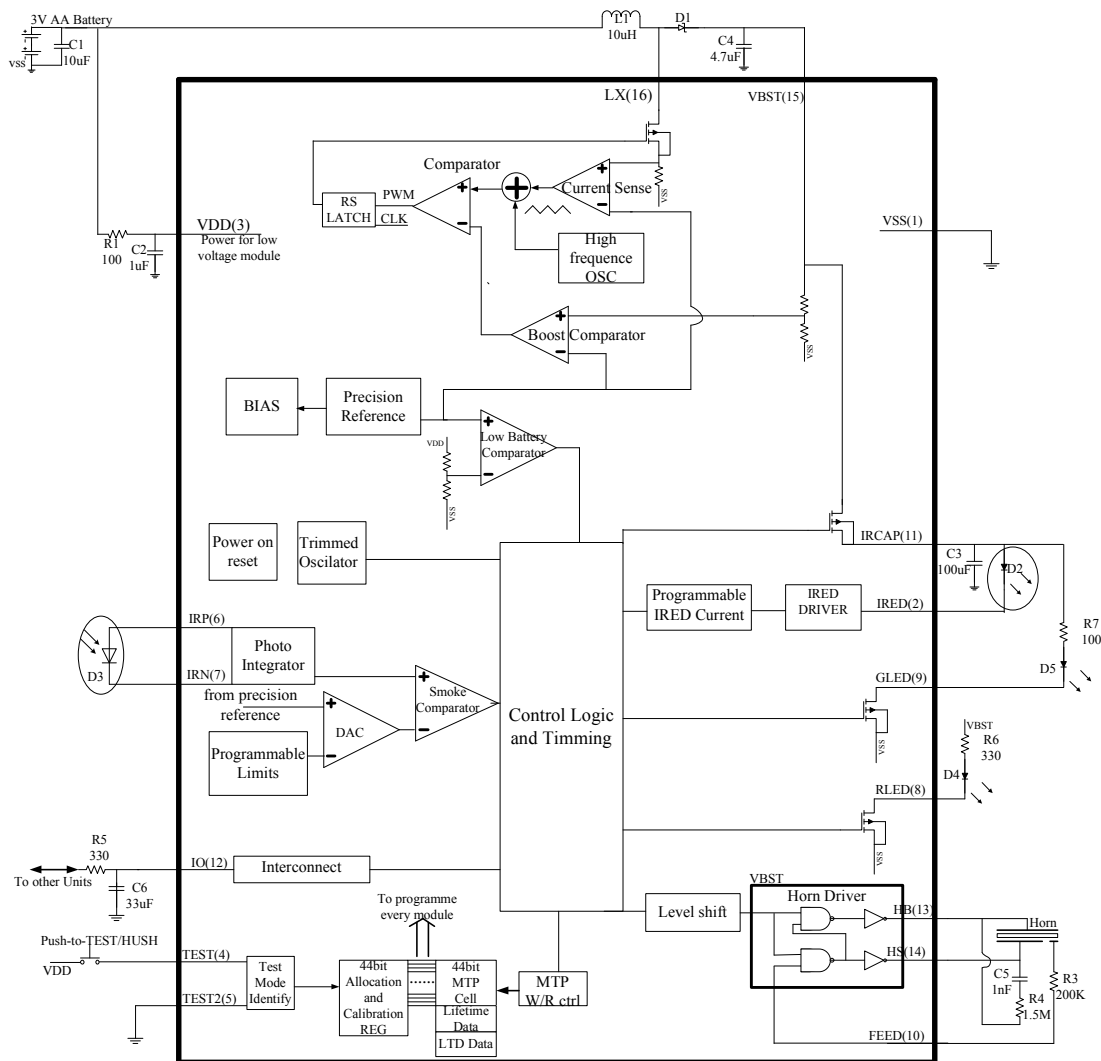
An interconnect pin allows multiple detectors to be connected such that, when one unit alarms, all units will sound.

the BL5980 was designed for use in smoke detectors that comply with Underwriters Laboratory Specification UL217 and UL268.

1.4 Ordering Information

Order Number	Package Type	Marking	Packing
BL5980	SOP-16	BL5980 XXXXX	Reel Tape
			Tube

1.5 Typical Application Circuit



Note

- 1: C2 should be located as close as possible to the device power pins, and C1 should be located as close as possible to VSS.
- 2: R3, R4 and C5 are typical values and may be adjusted to maximize sound pressure.
- 3: Schottky diode D1 must have a maximum peak current rating of at least 1.5A. For best results it should have forward voltage specification of less than 0.5V at 1A, and low reverse leakage.
- 4: Inductor L1 must have a maximum peak current rating of at least 1.5A.
- 5: DC-DC converter in High Boost mode (nominal VBST = 9.6V) can draw current pulses of greater than 1A, and is therefore very sensitive to series resistance. Critical components of this resistance are the inductor DC resistance, the internal resistance of the battery and the resistance in the connections from the inductor to the battery, from the inductor to the LX pin and from the VSS pin to the battery. In order to function properly under full load at VDD = 2V, the total of the inductor and interconnect resistances should not exceed 0.3Ω. The internal battery resistance should be no more than 0.5Ω, and a low ESR capacitor of 10 μF or more should be connected in parallel with the battery, to average the current draw over the boost converter cycle.

2.0. ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Supply Voltage $V_{DD}=5.5V$; $V_{BST}=13V$
 Input Voltage Range Except FEED, TEST..... $V_{IN} = -0.3V$ to $V_{DD} + 0.3V$
 FEED Input Voltage Range..... $V_{INFD} = -10$ to $+22V$
 TEST Input Voltage Range $V_{INTEST} = -.3V$ to $V_{BST}+.3V$
 Input Current except FEED..... $I_{IN} = 10$ mA
 Continuous Operating Current (HS, HB, V_{BST}).. $I_O= 40$ mA
 Continuous Operating Current (IRED) $I_{OIR}= 300$ mA
 Operating Temperature $T_A = -10$ to $+60^{\circ}C$
 Storage Temperature $T_{STG} = -55$ to $+125^{\circ}C$

Notice:

Stresses above those listed under "Maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability

2.2 DC Electrical Characteristics

DC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10$ to $+60^{\circ}C$, $V_{DD} = 3V$, $V_{BST} = 4.2V$, Typical Application (unless otherwise noted)(Note 1, Note 2, Note 3)

Parameter	Symbol	Test Pin	Min	Typ	Max	Units	Conditions
Supply Voltage	V_{DD}	3	2		5	V	Operating
Supply Current	I_{DD1}	3		1	2	μA	Standby, Inputs low, No loads, Boost Off, No smoke check
Standby Boost Current	I_{BST1}	15		100		nA	Standby, Inputs low, No loads, Boost Off, No smoke check
IRCAP Supply Current	I_{IRCAP}	11		500		μA	During smoke check
Boost Voltage	V_{BST1}	15	3	3.6	4.2	V	IRCAP charging for Smoke Check, GLED operation $I_{OUT} = 40$ mA
	V_{BST2}	15	8.5	9.6	10.7	V	No local alarm, RLED Operation, $I_{OUT} = 40$ mA, IO as an input
Input Leakage	I_{INOP}	6	-200		200	pA	$IRP = V_{DD}$ or V_{SS}
		7	-200		200	pA	$IRP = V_{DD}$ or V_{SS}
	I_{IHF}	10		20	50	μA	FEED = 22V; $V_{BST} = 9V$
	I_{ILF}	10	-50	-15		μA	FEED = -10V; $V_{BST} = 10.7V$

Input Voltage Low	V_{IL1}	10			2.7	V	FEED, $V_{BST} = 9V$
	V_{IL2}	12			800	mV	No local alarm, IO as an input
IO Hysteresis	V_{HYST1}	12		150		mV	
Input Pull Down Current	I_{PD1}	4,5	3	10	30	μA	$V_{IN} = V_{DD}$
	I_{PDIO1}	12	20		80	μA	$V_{IN} = V_{DD}$
	I_{PDIO2}	12			140	μA	$V_{IN} = 15V$
Output Voltage Low	V_{OL1}	13,14			500	mV	
	V_{OL2}	8			300	mV	
	V_{OL3}	9			300	mV	
Output High Voltage	V_{OH1}	13,14	8.5			V	$I_{OL} = 16\text{ mA}$, $V_{BST} = 9V$
Output Current	I_{IOH1}	12	-4	-5		mA	Alarm, $V_{IO} = 3V$ or $V_{IO} = 0V$, $V_{BST} = 9V$
	I_{IODMP}	12	5	15		mA	At Conclusion of Local Alarm or Test, $V_{IO}=1V$
	I_{IRED50}	2	45	50	55	mA	IRED on, $V_{IRED} = 1V$, $V_{BST} = 5V$, $I_{RCAP} = 5V$, (50 mA option selected; $T_A = 27^\circ C$)
	$I_{IRED100}$	2	90	100	110	mA	IRED on, $V_{IRED} = 1V$, $V_{BST} = 5V$, $I_{RCAP} = 5V$, (100 mA option selected; $T_A = 27^\circ C$)
	$I_{IRED150}$	2	135	150	165	mA	IRED on, $V_{IRED} = 1V$, $V_{BST} = 5V$, $I_{RCAP} = 5V$, (150 mA option selected; $T_A = 27^\circ C$)
	$I_{IRED200}$	2	180	200	220	mA	IRED on, $V_{IRED} = 1V$, $V_{BST} = 5V$, $I_{RCAP} = 5V$, (200 mA option selected; $T_A = 27^\circ C$)
IRED Current Temperature Coefficient	TC_{IRED}				0.5	%/ $^\circ C$	$V_{BST} = 5V$, $I_{RCAP} = 5V$; Note 4
Low Battery Alarm Voltage	V_{LB1}	3	2.05	2.1	2.15	V	Falling Edge; 2.1V nominal selected
	V_{LB2}	3	2.15	2.2	2.25	V	Falling Edge; 2.2V nominal selected
	V_{LB3}	3	2.25	2.3	2.35	V	Falling Edge; 2.3V nominal selected
	V_{LB4}	3	2.35	2.4	2.45	V	Falling Edge; 2.4V nominal selected
	V_{LB5}	3	2.45	2.5	2.55	V	Falling Edge; 2.5V nominal selected
	V_{LB6}	3	2.55	2.6	2.65	V	Falling Edge; 2.6V nominal selected

	V_{LB7}	3	2.65	2.7	2.75	V	Falling Edge; 2.7V nominal selected
	V_{LB8}	3	2.75	2.8	2.85	V	Falling Edge; 2.8V nominal selected
Low Battery Hysteresis	V_{LBHYST}	3		100		mV	

Note:

1: Wherever a specific VBST value is listed under test conditions, the VBST is forced externally with the inductor disconnected and the DC-DC converter NOT running.

2: Typical values are for design information only.

3: Limits over the specified temperature range are not production tested and are based on characterization data. Unless otherwise stated, production test is at room temperature with guard-banded limits.

4: Not production tested.

2.3 AC Electrical Characteristics

AC Electrical Characteristics: Unless otherwise indicated, all parameters apply at $T_A = -10^{\circ}\text{C}$ to $+60^{\circ}\text{C}$, $V_{DD} = 3\text{V}$, $V_{BST} = 4.2\text{V}$, Typical Application (unless otherwise noted) (Note 1 to Note 4).

Parameter	Symbol	Test Pin	Min	Typ	Max	Units	Conditon
Time Base							
Internal Clock Period	T _{PCLK}		9.8	10.4	11	ms	PROGSET, IO = high
RLED Indicator							
On Time	T _{ON1}	8	9.8	10.4	11	ms	Operating
Standby Period	T _{PLED1}	8	320	344	368	s	Standby, no alarm
Local Alarm Period	T _{PLED2A}	8	470	500	530	ms	Local alarm condition with temporal horn pattern
	T _{PLED2B}	8	625	667	710	ms	Local alarm condition with continuous horn pattern
Hush Timer Period	T _{PLED4}	8	10	10.7	11.4	s	Timer mode, no local alarm
External Alarm Period	T _{PLED0}	8	LED IS NOT ON			s	Remote alarm only
GLED Indicator							
Latched Alarm Period	T _{PLED3}	9	40	43	46	s	Latched Alarm Condition, LED enabled
Latched Alarm Pulse Train (3x) Off Time	T _{OFLED}	9	1.25	1.33	1.41	s	Latched Alarm Condition, LED enabled
Latched Alarm LED Enabled Duration	T _{LALED}	9	22.4	23.9	25.3	Hours	Latched Alarm Condition, LED enabled
Smoke Check							

Smoke Test Period with Temporal Horn Pattern	T _{PER0A}	2	10	10.7	11.4	s	Standby, no alarm
	T _{PER1A}	2	1.88	2	2.12	s	Standby, after one valid smoke sample
	T _{PER2A}	2	0.94	1	1.06	s	Standby, after two consecutive valid smoke samples
	T _{PER3A}	2	0.94	1	1.06	s	Local Alarm (three consecutive valid smoke samples)
	T _{PER4A}	2	235	250	265	ms	Push button test, >1 chamber detections
			313	333	353	ms	Push button test, no chamber detections
	T _{PER5A}	2	7.5	8	8.5	s	In remote alarm
Smoke Test Period with Continuous Horn Pattern	T _{PER0B}	2	10	10.7	11.4	s	Standby, no alarm
	T _{PER1B}	2	2.5	2.7	2.9	s	Standby, after one valid smoke sample
	T _{PER2B}	2	1.25	1.33	1.41	s	Standby, after two consecutive valid smoke samples
	T _{PER3B}	2	1.25	1.33	1.41	s	Local Alarm (three consecutive valid smoke samples)
	T _{PER4B}	2	313	333	353	ms	Push button test
	T _{PER5B}	2	10	10.7	11.4	s	In remote alarm
Chamber Test Period	T _{PCT1}	2	40	43	46	s	Standby, no alarm
Long Term Drift Sample Period	T _{LTD}	2	630	680	730	s	Standby, no alarm LTD enabled
Low Battery							
Low Battery Sample Period	T _{PLB1}	3	320	344	368	s	RLED on
	T _{PLB2}	3	80	86	92	s	RLED on
Horn Operation							
Low Battery Horn Period	T _{HPER1}	13	40	43	46	s	Low battery, no alarm
Chamber Fail Horn Period	T _{HPER2}	13	40	43	46	s	Chamber failure
Low Battery Horn On Time	T _{HON1}	13	9.8	10.4	11	ms	Low battery, no alarm
Chamber Fail Horn On Time	T _{HON2}	13	9.8	10.4	11	ms	Chamber failure
Chamber Fail Off Time	T _{HOF1}	13	305	325	345	ms	Failed chamber, no alarm, 3x chirp option
Alarm On Time with Temporal Horn Pattern	T _{HON2A}	13	470	500	530	ms	Local or remote alarm (Note 1)

Alarm Off Time with Temporal Horn Pattern	T_{HOF2A}	13	470	500	530	ms	Local or remote alarm (Note 1)
	T_{HOF3A}	13	1.4	1.5	1.6	s	Local or remote alarm (Note 1)
Alarm On Time with Continuous Horn Pattern	T_{HON2B}	13	235	250	265	ms	Local or remote alarm (Note 1)
Alarm Off Time with Continuous Horn Pattern	T_{HOF2B}	13	78	83	88	ms	Local or remote alarm (Note 1)
Push-to-Test Alarm Memory On Time	T_{HON4}	13	9.8	10.4	11	ms	Alarm memory active, push-to-test
Push-to-Test Alarm Memory Horn Period	T_{HPER4}	13	235	250	265	ms	Alarm memory active, push-to-test
Interconnect Signal Operation (IO)							
IO Active Delay	T_{IODLY1}	12		0		s	From start of local alarm to IO active
Remote Alarm Delay with Temporal Horn Pattern	$T_{IODLY2A}$	12	0.78	1	1.25	s	No local alarm, from IO active to alarm
Remote Alarm Delay with Continuous Horn Pattern	$T_{IODLY2B}$	12	380	572	785	ms	No local alarm, from IO active to alarm
IO Charge Dump Duration	T_{IODMP}	12	1.23	1.31	1.39	s	At conclusion of local alarm or test
IO Filter	T_{IOFILT}	12			313	ms	Standby, no alarm
Hush Timer Operation							
Hush Timer Period	T_{TPER}		8	8.6	9.1	Min	No alarm
Low Battery Hush Timer Period	T_{TPERLB}		7.73	8.22	8.71	Hours	No alarm
EOL							
End-of-Life Age Sample	T_{EOL}		314	334	354	Hours	EOL Enabled; Standby
Detection							
IRED On Time	T_{IRON}	2		100		μs	Prog Bits 3,4 = 1,1
		2		200		μs	Prog Bits 3,4 = 0,1
		2		300		μs	Prog Bits 3,4 = 1,0
		2		400		μs	Prog Bits 3,4 = 0,0

Note:

- 1: See timing diagram for Horn Pattern (Figure 5-2).
- 2: TPCLK and TIRON are 100% production tested. All other AC parameters are verified by functional testing.
- 3: Typical values are for design information only.
- 4: Limits over the specified temperature range are not production tested, and are based on characterization data.

2.4 Temperature Characteristics

Parameters	Sym	Min	Typ	Max	Units
Operating Temperature Range	TA	-10		60	°C
Storage Temperature Range	TSTG	-55		125	°C

3.0. PIN DESCRIPTIONS

3.1 Pin Function Table

Pin No.	Symbol	Function
1	VSS	Connect to the negative supply voltage.
2	IREL	Provides a regulated and programmable pulsed current for the infrared emitter diode.
3	VDD	Connect to the positive supply or battery voltage.
4	TEST	This input is used to invoke Test modes and the Timer mode. This input has an internal pull-down.
5	TEST2	Test input for test and programming modes. This input has an internal pull-down.
6	IRP	Connect to the anode of the photo diode.
7	IRN	Connect to the cathode of the photo diode.
8	RLED	Open drain NMOS output, used to drive a visible LED. This pin provides load current for the low battery test, and is a visual indicator for Alarm and Hush modes.
9	GLED	Open drain NMOS output used to drive a visible LED to provide visual indication of an Alarm Memory condition.
10	FEED	Usually connected to the feedback electrode through a current limiting resistor. If not used, this pin must be connected to VDD or VSS.
11	IRCAP	Used to charge and monitor the IRED capacitor.
12	IO	This bidirectional pin provides the capability to interconnect many detectors in a single system. This pin has an internal pull-down device and a charge dump device.
13	HB	This pin is connected to the metal electrode of a piezoelectric transducer.
14	HS	This pin is a complementary output to HB, connected to the ceramic electrode of the piezoelectric transducer.
15	VBST	Boosted voltage produced by DC-DC converter.

16	LX	Open drain NMOS output, used to drive the boost converter inductor. The inductor should be connected from this pin to the positive supply through a low resistance path.
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4.0. DEVICE DESCRIPTION

4.1 Standard Internal Timing

The internal oscillator is trimmed to $\pm 6\%$ tolerance. Once every 10 seconds, the boost converter is powered up, the IRCAP is charged from VBST and then the detection circuitry is active for 10 ms. Prior to completion of the 10 ms period, the IRED pulse is active for a user-programmable duration of 100-400 μ s. During this IRED pulse, the photo diode current is integrated and then digitized. The result is compared to a limit value stored in MTP during calibration to determine the photo chamber status. If a smoke condition is present, the period to the next detection decreases, and additional checks are made.

4.2 Smoke Detection Circuit

The digitized photo amplifier integrator output is compared to the stored limit value at the conclusion of the IRED pulse period. The IRED drive is all internal, and both the period and current are user programmable. Three consecutive smoke detections will cause the device to go into Alarm and activate the horn and interconnect circuits. In Alarm, the horn is driven at the high boost voltage level, which is regulated based on an internal voltage reference, and therefore results in consistent audibility over battery life. RLED will turn on for 10 ms at a 2 Hz rate. In Local Alarm, the integration limit is internally decreased to provide alarm hysteresis.

The integrator has three separate gain settings:

- Normal and Hysteresis
- Reduced Sensitivity (HUSH)
- High Gain for Chamber Test and Push-to-Test

There are four separate sets of integration limits (all user programmable):

- Normal Detection
- Hysteresis
- HUSH
- Chamber Test and Push-to-Test modes

In addition, there are user selectable integrator gain settings to optimize detection levels (see Table 4-1).

4.3 Supervisory Test

Once every 86 seconds, the status of the battery voltage is checked by enabling the boost converter for 10 ms and comparing a fraction of the VDD voltage to an internal reference. In each period of 344 seconds, the battery voltage is checked four times. Three checks are unloaded and one check is performed with the RLED enabled, which provides a battery load. The High Boost mode is active only for the loaded low battery test. In addition, once every 43 seconds the chamber is activated and a High Gain mode and chamber test limits are internally selected. A check of the chamber is made by amplifying background reflections. The Low Boost mode is used for the chamber test.

If either the low battery test or the chamber test fails, the horn will pulse on for 10 ms every 43 seconds, and will continue to pulse until the failing condition passes. If two consecutive chamber tests fail, the horn will pulse on three times for 10 ms, separated by 330 ms every 43 seconds. Each of the two supervisory test audible indicators is separated by approximately 20 seconds.

As an option, a Low Battery Silence mode can be invoked. If a low battery condition exists, and

the TEST input is driven high, the RLED will turn on. If the TEST input is held for more than 0.5 second, the unit will enter the Push-to-test operation described in Section 4.4 “Push-to-Test Operation (PTT)”. After the TEST input is driven low, the unit enters in Low Battery Hush mode, and the 10 ms horn pulse is silenced for 8 hours. The activation of the test button will also initiate the 9 minute Reduced Sensitivity mode described in Section 4.6 “Reduced Sensitivity Mode”. At the end of the 8 hours, the audible indication will resume if the low battery condition still exists.

4.4 Push-to-Test Operation (PTT)

If the TEST input pin is activated (VIH), the smoke detection rate increases to once every 250 ms after one internal clock cycle. In Push-to-Test, the photo amplifier High Gain mode is selected, and background reflections are used to simulate a smoke condition. After the required three consecutive detections, the device will go into a Local Alarm condition. When the TEST input is driven low (VIL), the photo amplifier Normal Gain is selected, after one clock cycle. The detection rate continues at once every 250 ms until three consecutive No Smoke conditions are detected. At this point, the device returns to standby timing. In addition, after the TEST input goes low, the device enters the HUSH mode (see Section 4.6 “Reduced Sensitivity Mode”).

4.5 Interconnect Operation (I/O)

The bidirectional IO pin allows the interconnection of multiple detectors. In a Local Alarm condition, this pin is driven high (High Boost) immediately through a constant current source. Shorting this output to ground will not cause excessive current. The IO is ignored as input during a Local Alarm.

The IO pin also has an NMOS discharge device that is active for 1.3 seconds after the conclusion of any type of Local Alarm. This device helps to quickly discharge any capacitance associated with the interconnect line.

If a remote, active high signal is detected, the device goes into Remote Alarm and the horn will be active. RLED will be off, indicating a Remote Alarm condition. Internal protection circuitry allows the signaling unit to have a higher supply voltage than the signaled unit, without excessive current draw.

The interconnect input has a 336 ms nominal digital filter. This allows the interconnection to other types of alarms (carbon monoxide, for example) that may have a pulsed interconnect signal.

4.6 Reduced Sensitivity Mode

A Reduced Sensitivity or Hush mode is initiated by activating the TEST input (VIH). If the TEST input is activated during a Local Alarm, the unit is immediately reset out of the alarm condition, and the horn is silenced. When the TEST input is deactivated (VIL), the device enters into a 9-minute nominal Hush mode. During this period, the HUSH integration limit is selected. The hush gain is user programmable. In Reduced Sensitivity mode, the RLED flashes for 10 ms every 10 seconds to indicate that the mode is active. As an option, the Hush mode will be cancelled if any of the following conditions exist:

- Reduced sensitivity threshold is exceeded (high smoke level)
- An interconnect alarm occurs
- TEST input is activated again.

4.7 Local Alarm Memory

An Alarm Memory feature allows easy identification of any unit that had previously been in a Local Alarm condition. If a detector has entered a Local Alarm, when it exits that Local Alarm, the Alarm Memory latch is set. Initially the GLED can be used to visually identify any unit that

had previously been in a Local Alarm condition. The GLED flashes three times spaced 1.3 seconds apart. This pattern will repeat every 43 seconds. The duration of the flash is 10 ms. In order to preserve battery power, this visual indication will stop after a period of 24 hours. The user will still be able to identify a unit with an active alarm memory by pressing the Push-to-Test button. When this button is active, the horn will chirp for 10 ms every 250 ms. If the Alarm Memory condition is set, then any time the Push-to-Test button is pressed and released, the Alarm Memory latch is reset. The initial 24 hour visual indication is not displayed if a low battery condition exists.

4.8 End-of-Life Indicator

As an option, after every 14 days of continuous operation, the device will read a stored age count from the MTP and increment this count. After 10 years of powered operation, an audible warning will occur indicating that the unit should be replaced. This indicator will be similar to the chamber test failure warning in that the horn will pulse on three times for 10 ms separated by 330 ms every 43 seconds. This indicator will be separated from the low battery indicator by approximately 20 seconds.

4.9 Photo Chamber Long Term Drift Adjustment

As an option, the design includes a Long Term Drift Adjustment for the photo chamber. If this option is selected, during calibration a normal no-smoke baseline integration measurement is made and stored in MTP. During normal operation, a new baseline is calculated by making 64 integration measurements over a period of 12 hours. These measurements are averaged and compared to the original baseline stored during calibration to calculate the long term drift. All four limits stored during calibration are adjusted by this drift factor. Drift sampling is suspended during Hush, Local Smoke and Remote Smoke conditions.

5.0. USER PROGRAMMING MODES

TABLE 5-1: PARAMETRIC PROGRAMMING

Parametric Programming		Range		Resolution	
IRED Period		100–400 μ s		100 μ s	
IRED Current Sink		50–200 mA		50 mA	
Low Battery Detection Voltage		2.1 – 2.8V		100 mV	
Photo Detection Limits		Typical Maximum Input Current (nA)			
		100 μ s	200 μ s	300 μ s	400 μ s
Normal/Hysteresis	GF = 1	58	29	19.4	14.5
	GF = 2	29	14.5	9.6	7.2
	GF = 3	14.5	7.2	4.8	3.6
	GF = 4	7.2	3.6	2.4	1.8
Hush	GF = 1	116	58	38.8	29
	GF = 2	58	29	19.4	14.5
	GF = 3	29	14.5	9.6	7.2
	GF = 4	14.5	7.2	4.8	3.6
Chamber Test	GF = 1	29	14.5	9.6	7.2
	GF = 2	14.5	7.2	4.8	3.6
	GF = 3	7.2	3.6	2.4	1.8
	GF = 4	3.6	1.8	1.2	0.9

Note:

1: GF is the user selectable Photo Integration Gain Factor. Once selected, it applies to all modes of operation. For example, if GF = 1 and integration time is selected to be 100 μ s, the ranges will be as follows: Normal/Hysteresis = 58 nA, Hush = 116 nA, Chamber Test = 29 nA.

2: Nominal measurement resolution in each case will be 1/63 of the maximum input range.

3: The same current resolution and ranges applies to the limits.

TABLE 5-2: FEATURES PROGRAMMING

Features	Options
Tone Select	Continuous or NFPA Tone
10 Year End-of-life Indicator	Enable/Disable
Photo Chamber Long Term Drift Adjustment	Enable/Disable
Low Battery Hush	Enable/Disable
Hush Options	Option 1: Hush mode is not cancelled for any reason. If the test button is pushed during Hush, the unit reverts to Normal Sensitivity to test the unit, but when it comes out of test, resumes in Hush where it left off.
Option 2: The Hush mode is cancelled if the Reduced Sensitivity threshold is exceeded (high smoke level), and if an external (interconnect alarm) is signaled. If the test button is pushed during Hush, after the test is executed, the Hush mode is terminated.	

5.1 Calibration and Programming Procedures

Thirteen separate programming and test modes are available for user customization. To enter these modes, after power-up, TEST2 must be driven to VDD and held at that level. The TEST input is then clocked to step through the modes. FEED and IO are reconfigured to become test mode inputs, while RLED, GLED and HB become test mode outputs. The test mode functions for each pin are outlined in Table 5-3.

TABLE 5-3: TEST MODE FUNCTIONS

Mode	Description	TEST Clock	TEST Data	TEST2	FEED	IO	RLED	GLED	HB
	VIH	VBST	VDD	VDD	VBST	VDD	—	—	—
	VIL	VSS	VSS	VSS	VSS	VSS	—	—	—
T0	Horn Test	0	HornEn	VDD	FEED	IO	RLED	GLED	HB
T1	Low Battery test	1	not used	VDD	BoostEn	LBstrb	RLEDen	GLEDen	LBout
T2	Photo Gain Factor(2bits)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Integ Time (2bits)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	IREC Current (2bits)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Low Battery Trip (3bits)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	LTD Enable (1bit)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Hush Option (1bit)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	LB Hush Enable (1bit)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	EOL Enable(1bit)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
	Tone Select (1bit)	2	ProgData	VDD	ProgCLK	ProgEn 14 bits	RLED	GLED	HB
T3	Norm Lim Set (6bits)	3	not used	VDD	CalCLK	IntLat(3)	Gamp	IntegOut	SmkComp(1)
T4	Hyst Lim Set (6bits)	4	not used	VDD	CalCLK	IntLat(3)	Gamp	IntegOut	SmkComp(1)
T5	Hush Lim Set (6bits)	5	not used	VDD	CalCLK	IntLat(3)	Gamp	IntegOut	SmkComp(1)
T6	Ch Test Lim Set(6bits)	6	not used	VDD	CalCLK	IntLat(3,4)/ProgEn 24 bits	Gamp	IntegOut	SmkComp(1)
T7	Serial Read/Write	7	ProgData	VDD	ProgCLK	ProgEn	RLED	GLED	Serial Out
T8	LTD Baseline (6 bits)	8	not used	VDD	MeasEn	ProgEn 30 bits	Gamp	IntegOut	HB
T9	Norm Lim Check	9	not used	VDD	MeasEn	not used	Gamp	IntegOut	SCMP(2)
T10	Hyst Lim Check	10	not used	VDD	MeasEn	not used	Gamp	IntegOut	SCMP(2)
T11	Hush Lim Check	11	not used	VDD	MeasEn	not used	Gamp	IntegOut	SCMP(2)
T12	Ch Test Lim Check	12	not used	VDD	MeasEn	not used	Gamp	IntegOut	SCMP(2)

Note

- 1: SmkComp (HB) - digital comparator output (high if Gamp < IntegOut; low if Gamp > IntegOut)
- 2: SCMP (HB) - digital output representing comparison of measurement value and associated limit. Signal is valid only after MeasEn has been asserted and measurement has been made. (SCMP high if measured value > limit; low if measured value < limit).
- 3: IntLat (IO) – digital input used for two purposes. If FEED is at a logic high level, then a low to high transition on IntLat will initiate an integration cycle. If FEED is at a logic low level, then a low to high transition on IntLat will latch the present state of the limits (GAMP level) for later storage. T2-T5 limits are latched, but not stored until ProgEn is asserted in T6 mode
- 4: At the end of T6 mode, in order to store the limits, the IO input must be pulsed twice consecutively with FEED held low. The first pulse will latch the data and the second will store it in MTP.

5.2 User Selections

Prior to smoke calibration, the user must program the functional options and parametric selections. This requires that 14 bits, representing selected values, be clocked in serially using TEST as a data input and FEED as a clock input, and then be stored in the internal MTP.

The detailed steps are as follows:

1. Power up with bias conditions as shown in Figure 5-1. At power-up TEST = TEST2 = FEED = IO = VSS.
2. Drive TEST2 input from VSS to VDD and hold at VDD through Step 5 below.
3. Using TEST as data and FEED as clock, shift in values as selected from Register 5-1. The minimum

pulse width for FEED is 10 μ s, while the minimum pulse width for TEST is 100 μ s. For example, for the following options, the sequence would be:

data - 0 0 0 1 1 0 0 0 1 0 0 0 0 1
bit - 30 31 32 33 34 35 36 37 38 39 40 41 42 43

Photo Amp Gain Factor = 1

Integration Time = 200 μ s

IRED Current = 100 mA

Low Battery Trip = 2.2V

Long Term Drift, Low Battery Hush and EOL are all disabled

Hush Option = Never Cancel

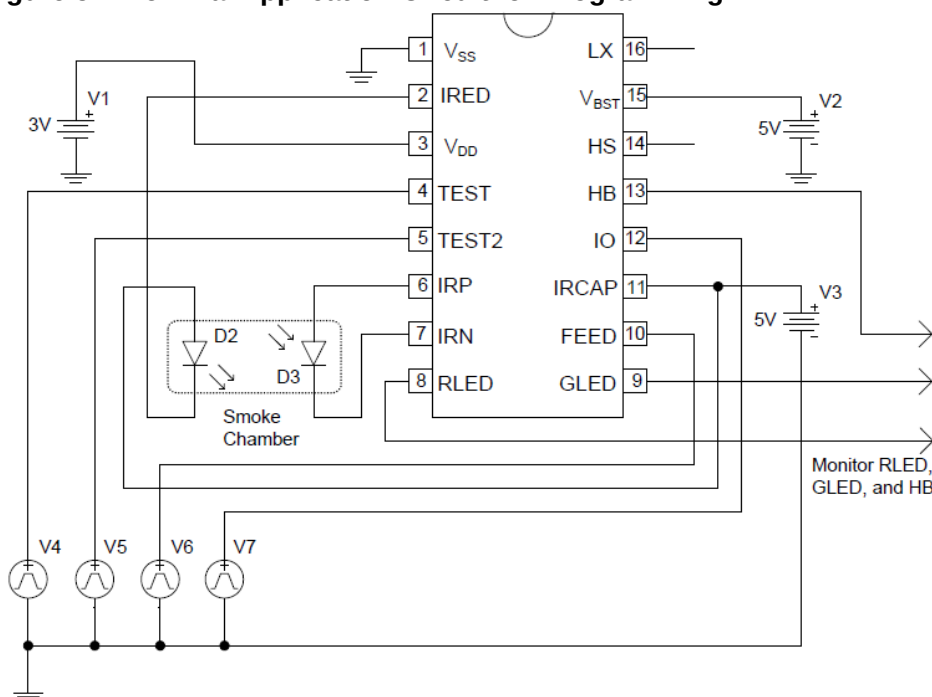
Tone Select = Temporal

4. After shifting in data, pull IO input to VDD, then VSS (minimum pulse width of 100ms) to store shift register contents into the memory.

5. If any changes are required, power down the part and return to Step 1. All bit values must be reentered.

Note: For test mode T2 only 14 bits (bits 25-38) will be loaded. For test mode T8 all 44 bits (bits 0-43), will be loaded.

Figure 5-1 Nominal Application Circuit for Programming



REGISTER 5-1 CONFIGURATION AND CALIBRATION SETTINGS REGISTER

				W	W	W	W
				TS	EOL	LBH	HUSH
				bit 43			bit 40

W	W	W	W	W	W	W	W
LTD	LB0	LB1	LB2	IRC1	IRC0	IT1	IT0
bit 39							bit 32

W	W	W	W	W	W	W	W
PAGF1	PAGF0	NL5	NL4	NL3	NL2	NL1	NL0
bit 31							bit 24

W	W	W	W	W	W	W	W
HYL5	HYL4	HYL3	HYL2	HYL1	HYL0	HUL5	HUL4
bit 23							bit 16

W	W	W	W	W	W	W	W
HUL3	HUL2	HUL1	HUL0	CTL5	CTL4	CTL3	CTL2
bit15							bit 8

W	W	W	W	W	W	W	W
CTL1	CTL0	LTD5	LTD4	LTD3	LTD2	LTD1	LTD0
bit 7							bit 0

Note: W=writable bit

- bit 43 **Tone Select**
 TS
 0=Continuous Horn Pattern
 1=Temporal Horn Pattern
- bit 42 **End of Life Enable**
 EOL
 0=Disable
 1=Enable
- bit 41 **Low Battery Hush Enable**
 LBH
 0=Disable
 1=Enable
- bit 40 **Hush Option**
 HUSH
 0=Never Cancel
 1=Cancelled for high smoke level, interconnect alarm, or second push of TEST button (as described above Low Battery Hush Enable)
- bit 39 **Long Term Drift Enable**
 LTD
 0=Disable
 1=Enable
- bit 38-36 **Low Battery Trip Point**
 LB0, LB1, LB2
 000=2.1V
 001=2.2V
 010=2.3V
 011=2.4V
 100=2.5V

101=2.6V

110=2.7V

111=2.8V

bit 35-34

ired Current

IRC1, IRC0

00=50mA

01=100mA

10=150mA

11=200mA

bit 33-32

Integration Time

IT1, IT0

00=400us

01=300us

10=200us

11=100us

bit 31-30

Photo Amplifier Gain Factor

PAGF1, PAGF0

00=1

01=2

10=3

11=4

bit 29~24

Normal Limits (Section 3.2)

NL5, NL4, NL3, NL2, NL1, NL0

000000=0

000001=1

...

111110=62

111111=63

bit 23-18

Hysteresis Limits (Section 3.2)

HYL5, HYL4, HYL3, HYL2, HYL1, HYL0

000000=0

000001=1

...

111110=62

111111=63

bit 17-12

Hush Limits (Section 3.6)

HUL5, HUL4, HUL3, HUL2, HUL1, HUL0

000000=0

000001=1

...

111110=62

111111=63

bit 11-6

Chamber Test Limits (Section 3.3)

CTL5, CTL4, CTL3, CTL2, CTL1, CTL0

000000=0

000001=1

...

111110=62

111111=63

bit 5-0

Long Tern Drift Sample (Section 3.9)

LTD5, LTD4, LTD3, LTD2, LTD1, LTD0

000000=0

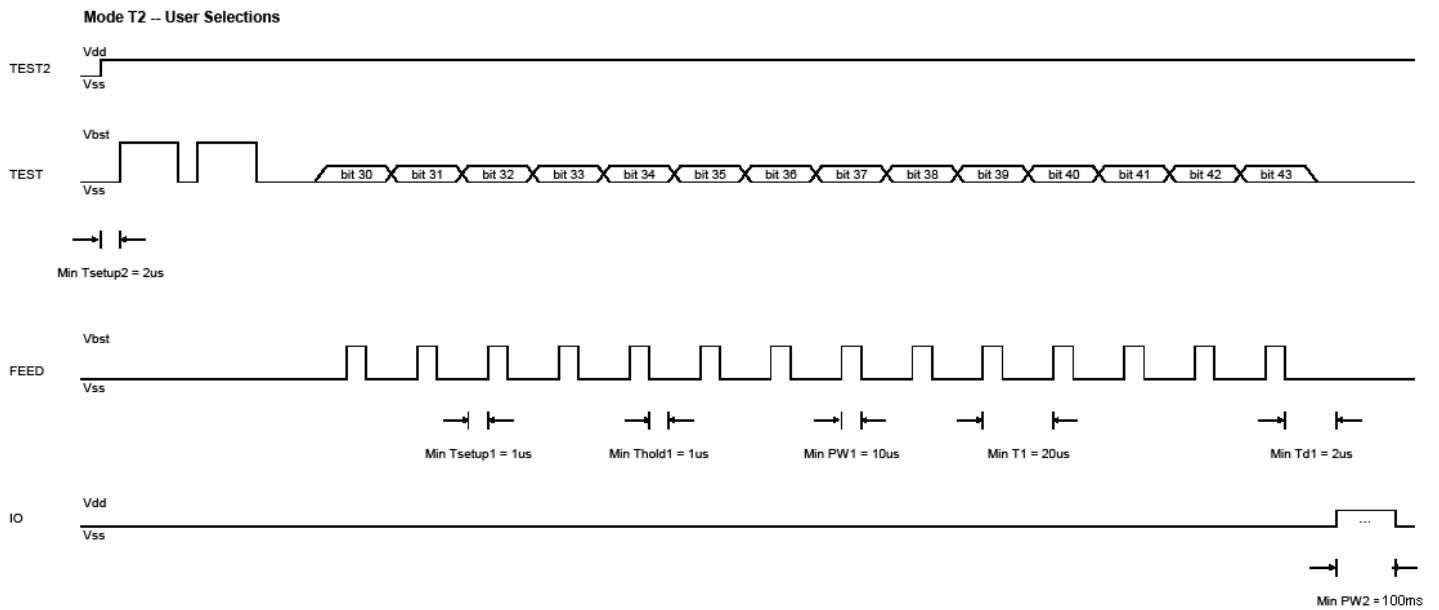
000001=1

...

111110=62

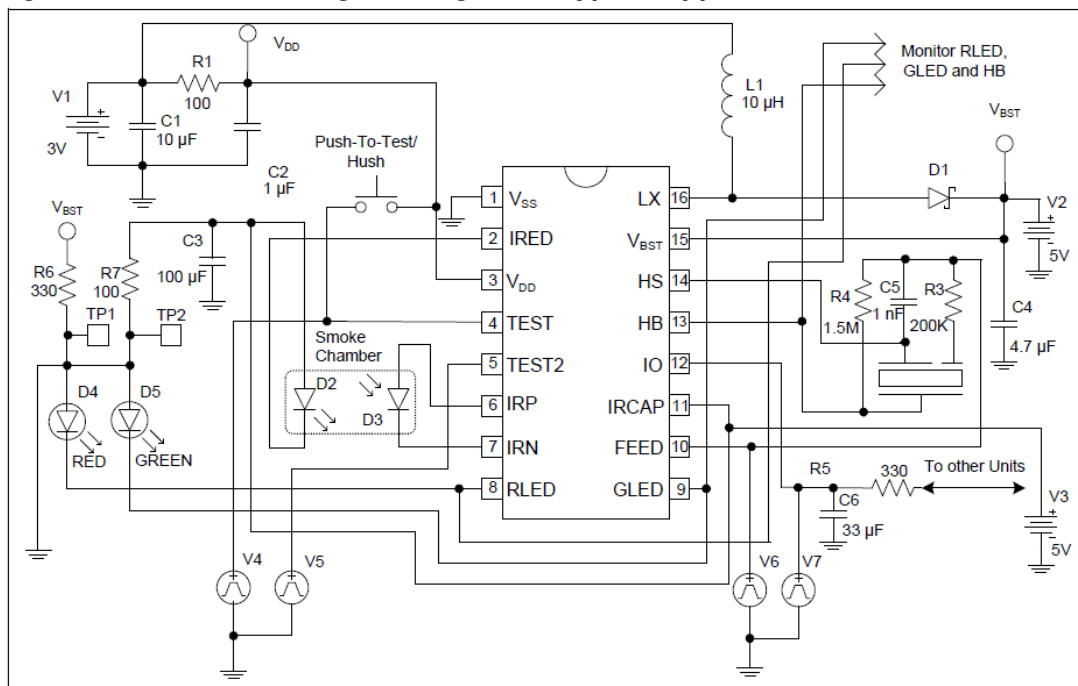
111111=63

Figure 5-2: Timing Diagram for Mode T2



As an alternative to Figure 5-1, Figure 5-3 can be used to program while in the application circuit. Note that in addition to the five programming supplies, connections to Vss are needed at TP1 and TP2.

Figure 5-3: Circuit for Programming in the Typical Application



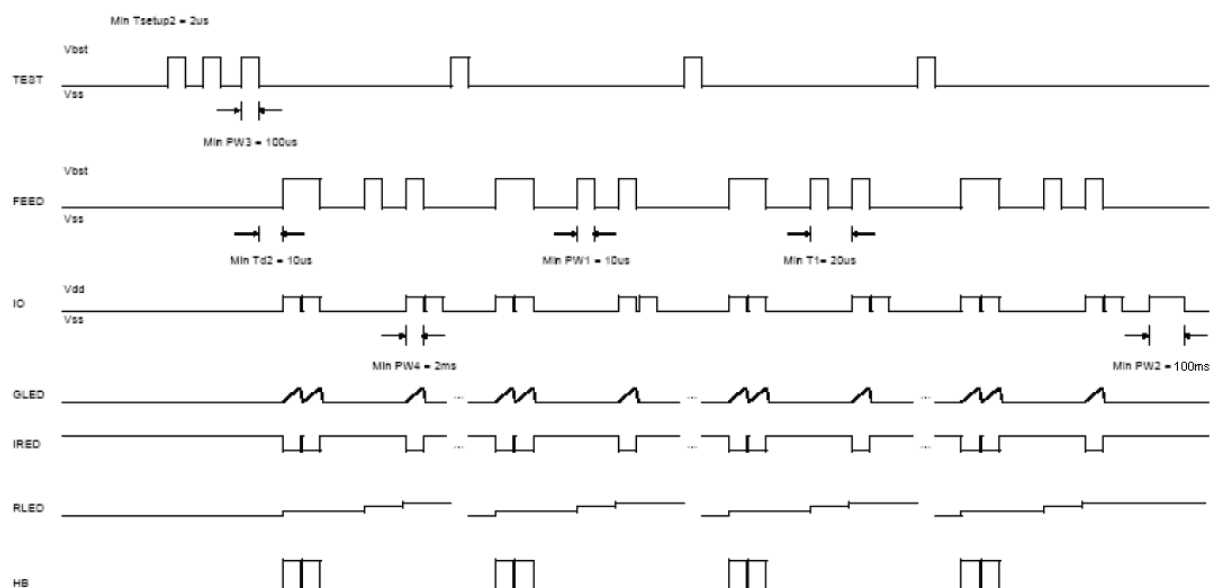
5.3 Smoke Calibration

A separate calibration mode is entered for each measurement mode (Normal, Hysteresis, Hush and Chamber Test) so that independent limits can be set for each. In all calibration modes, the integrator output can be accessed at the GLED output.

The Gamp output voltage, which represents the smoke detection level, can be accessed at the RLED output. The SmkComp output voltage is the result of the comparison of Gamp with the integrator output, and can be accessed at HB. The FEED input can be clocked to step up the smoke detection level at RLED. Once the desired smoke threshold is reached, the TEST input is pulsed low to high to store the result.

The procedure is described in the following steps:

1. Power up with the bias conditions shown in Figure 5-1.
2. Drive TEST2 input from VSS to VDD to enter the Programming mode. TEST2 should remain at VDD through Step 8 described below.
3. Apply three clock pulses to TEST input to enter T3 mode. This initiates the calibration mode for Normal Limits setting. The Integrator output should appear at GLED and the smoke detection level at RLED.
4. At this point clock FEED to increase the smoke detection level as needed. Pulling IO high with FEED to increase the smoke detection level as needed. Pulling IO high with FEED at a logic high level will initiate an integration. The integrator output signal should appear at GLED. The sequence of incrementing the limit, performing an integration and monitoring the HB output for the resulting comparison can be repeated until the desired threshold is reached. Once the desired smoke threshold is reached, with FEED held low, the IO input should be pulsed low to high to latch the smoke detection level.
5. Apply a fourth clock pulse to TEST input to enter T4 mode. This initiates the calibration mode for Hysteresis Limits. The sequence in Step 4 should be repeated to set the Hysteresis Limit.
6. Apply clock pulse to TEST input again to enter T5 mode and initiate calibration for Hush Limits. Repeat Step 4 to set the Hush Limit.
7. Apply clock pulse to TEST input a sixth time to enter T6 mode and initiate calibration for Chamber Test Limits. Repeat Step 4 to set the Chamber Test Limit.
8. After pulsing the IO input to latch the Chamber Test Limit, the IO must be pulsed low to high a second time to store the limits in memory.

Figure 5-4: Timing Diagram for Modes T3 to T6


5.4 Serial Read/Write

As an alternative to the steps in Section 5.3 “Smoke Calibration”, if the system has been well characterized, the limits and baseline can be entered directly from a serial read/write calibration mode.

To enter this mode, follow these steps:

1. Set up the application as shown in Figure 5-1.
2. Drive TEST2 input from VSS to VDD to enter in Programming mode. TEST2 should remain at VDD until all data has been entered.
3. Clock the TEST input to mode T8 (High = VBST, Low = VSS, 8 clocks). This enables the Serial Read/Write mode.
4. TEST now acts as a data input (High = VDD, Low = VSS). FEED acts as the clock input (High = VBST, Low = VSS). Clock in the limits, LTD baseline, functional and parametric options. The data sequence should be as follows:
 - 6 bit LTD sample (LSB first)
 - 6 bit Chamber Test Limits (LSB first)
 - 6 bit Hush Limits (LSB first)
 - 6 bit Hysteresis Limits (LSB first),
 - 6 bit Normal Limits (LSB first)

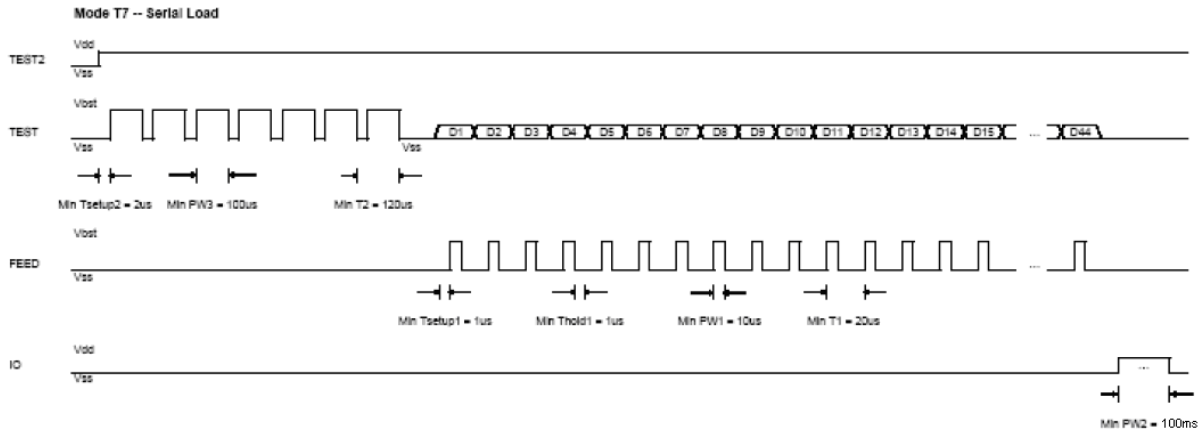
Then, the data sequence follows the pattern described in Register 5-1:

- 2 bit Photo Amp Gain Factor
- 2 bit Integration Time
- 2 bit IRED current
- 3 bit Low Battery Trip Point
- 1 bit Long Term Drift Enable
- 1 bit Hush Option
- 1 bit Low Battery Hush Enable
- 1 bit EOL enable
- 1 bit Tone Select

A serial data output is available at HB.

5. After all 44 bits have been entered, pulse IO to store into the MTP memory.

Figure 5-5: Timing Diagram for Mode T7

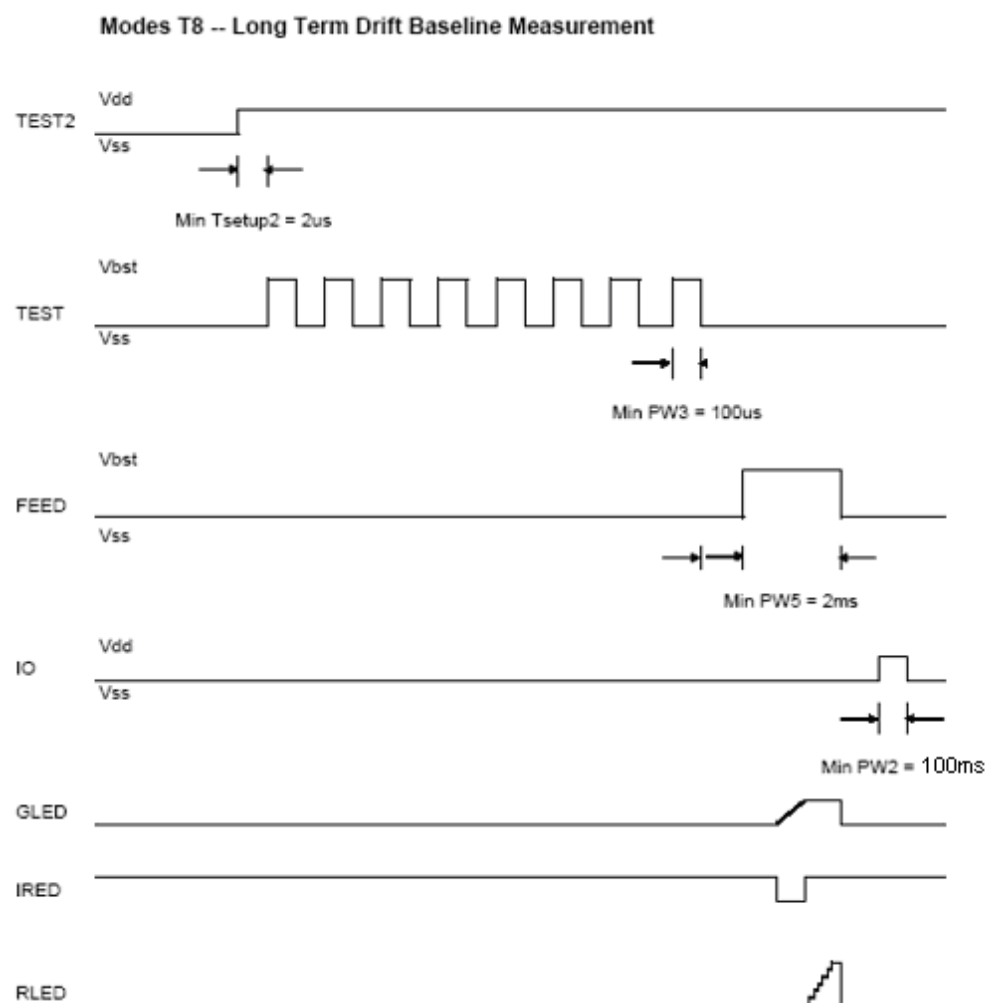


5.5 LTD Baseline Measurement

If the Long Term Drift Adjustment is enabled, a Long Term Drift Baseline must be set. If an accurate value is known based on previous chamber characterization, it can be loaded above in T7 with the serial data. If not, zeros can be entered as placeholders in T7 and a long term drift (LTD) baseline measurement must be made. To do this, the unit should be connected to its smoke chamber and placed in a no-smoke condition. To enable the baseline measurement, pull TEST from VSS to VBST again (or a total of 8 times) and return to VSS. Once the chamber is clear, pulse FEED low to high to make the baseline measurement. The duration of this pulse should be at least 2ms.

After baseline LTD measurement has been made, pulse IO with FEED held low to store the result in memory.

Figure 5-6: Timing Diagram for Mode T8

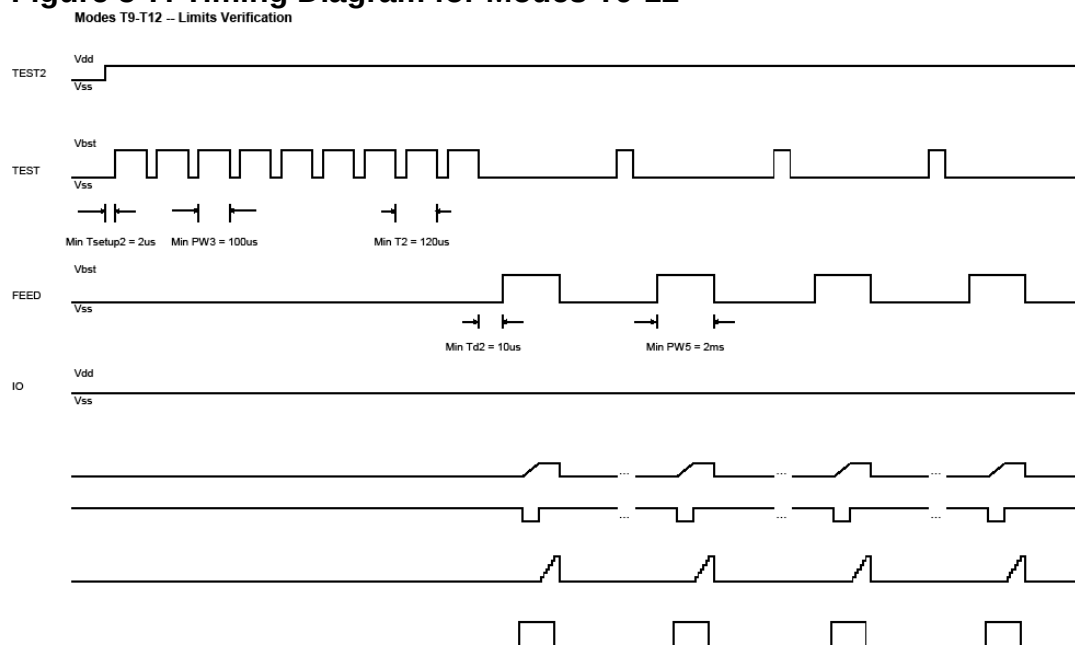


5.6 Limits Verification

After all limits and LTD baseline have been entered and stored into the memory, additional test modes are available to verify if the limits are functioning as expected. Table 5-4 describes several verification tests.

TABLE 5-4: LIMITS VERIFICATION DESCRIPTION

Limit	Test Description
Normal Limits	Clock TEST to Mode T9 (9 clocks). With appropriate smoke level in chamber, pull FEED to VDD and hold for at least 1 ms. The HB output will indicate the detection status (High = smoke detected).
Hysteresis Limits	Clock TEST to Mode T10 (10 clocks). Pulse FEED and monitor HB as in Normal Limits case.
Hush Limits	Clock TEST to Mode T11 (11 clocks). Pulse FEED and monitor HB.
Chamber Test Limits	Clock TEST to Mode T12 (12 clocks). Pulse FEED and monitor HB.

Figure 5-7: Timing Diagram for Modes T9-12


5.7 Horn Test

This mode allows the horn to be enabled indefinitely for audibility testing. To enable, the TEST2 input should be driven to the Vdd level and TEST should be held at Vss. The IO pin is configured as horn enable.

Figure 5-8: Timing Diagram for Mode T0


5.8 Low Battery Test

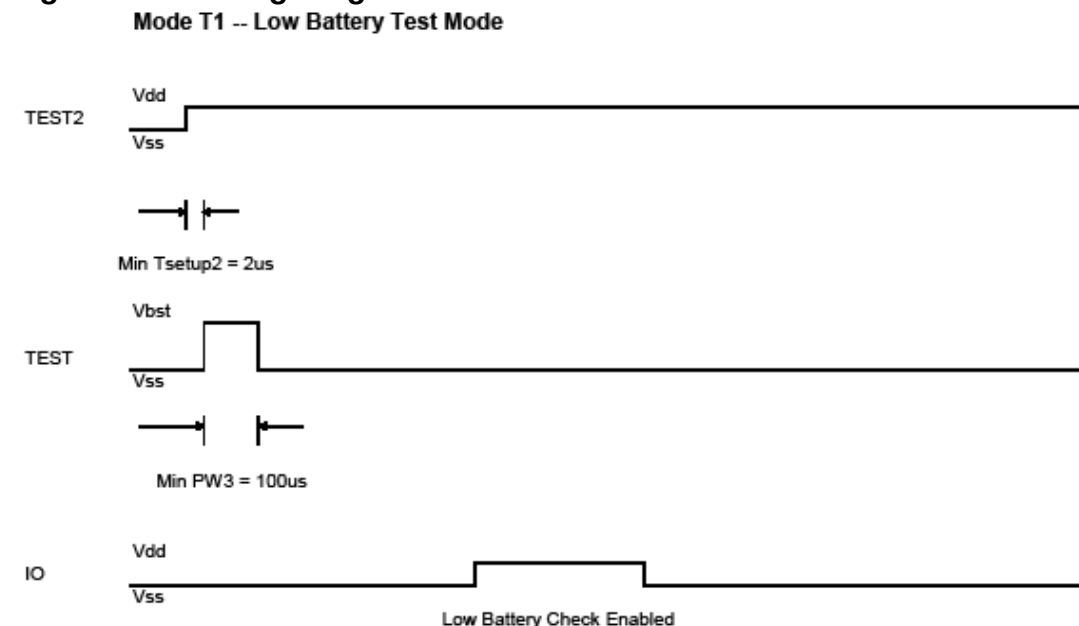
This mode allows the user to enable the internal low battery circuitry to perform a low battery test. To enter this mode, follow these steps:

1. Power up with the bias conditions shown in Figure 5-1.
2. Drive TEST2 input from VSS to VDD to enter the Programming mode. TEST2 should remain at Vdd through the following steps
3. Apply one clock pulse to the TEST input to enter the T1 mode
4. Drive the IO input from VSS to Vdd. This will enable the boost converter and turn on the RLED

driver.

5. Monitor the HB output for the low battery comparator status.

Figure 5-9: Timing Diagram for Mode T1



6.0. APPLICATION NOTES

6.1 Standby Current Calculation and Battery Life

The supply current shown in the **DC Electrical Characteristics** table is only one component of the average standby current and, in most cases, can be a small fraction of the total, because power consumption generally occurs in relatively infrequent bursts and depends on many external factors. These include the values selected for IRED current and integration time, the VBST and IR capacitor sizes and leakages, the VBAT level, and the magnitude of any external resistances that will adversely affect the boost converter efficiency.

A calculation of the standby current for the battery life is shown in Table 5-1, based on the following parameters:

VBAT = 3

VBST1 = 3.6

VBST2 = 9

Boost capacitor size = 4.70E-06

Boost Efficiency = 8.50E-01

IRED on time = 2.000E-04

IRED Current = 1.000E-01

TABLE 6-1: STANDBY CURRENT CALCULATION

IDD Component	Voltage (V)	Current (A)	Duration (s)	Energy (J)	Period (s)	Average Power (W)	IDD Contribution (A)	IBAT (uA)
Fixed IDD	3	1.00E-06	1			3.00E-06	1.00E-06	1.0
Photo Detection Current								
Chamber test	3.6	1.00E-03	1.0E-02	3.60E-05	43	9.85E-07	3.28E-07	0.3

(excluding IR drive)								
IR drive during Chamber Test	3.6	0.10	2.00E-04	7.20E-05	43	1.97E-06	6.57E-07	0.7
Smoke Detection (excluding IR drive)	3.6	1.00E-03	1.00E-02	3.60E-05	10.75	3.94E-06	1.31E-06	1.3
IR drive during Smoke Detection	3.6	0.10	2.00E-04	7.20E-05	10.75	7.88E-06	2.63E-06	2.6
Low Battery Check Current								
Loaded Test								
Load	9	2.00E-02	1.00E-02	1.80E-03	344.00	6.16E-06	2.05E-06	2.1
Boost	Vbst1 to Vbst2			6.85E-05	344.00	2.34E-07	7.81E-08	0.1
Unloaded Test								
Load	3.6	1.00E-04	1.00E-02	3.60E-06	43.00	9.85E-08	3.28E-08	0.0
						Total	8.09E-06	8.1

The following paragraphs explain the components in Table 6-1.

6.1.1 Fixed IDD

The IDD is the Supply Current shown in the DC Electrical Characteristics table.

6.1.2 PHOTO DETECTION CURRENT

Photo Detection Current is the current draw due to the smoke testing every 10.75 seconds, and the chamber test every 43 seconds. The current for both the IR diode and the internal measurement circuitry comes primarily from VBST, so the average current must be scaled for both on-time and boost voltage.

The contribution to IBAT is determined by first calculating the energy consumed by each component, given its duration. An average power is then calculated based on the period of the event and the boost converter efficiency (assumed to be 85% in this case). An IBAT contribution is then calculated based on this average power and the given VBAT. For example, the IR drive contribution during chamber test is detailed in Equation 6-1:

EQUATION 6-1:

$$\frac{3.6V \times 0.1A \times 200 \text{ us}}{43s \times 0.85 \times 3V} = 0.657 \text{ uA}$$

6.1.3 LOW BATTERY CHECK CURRENT

The Low Battery Check Current is the current required for the low battery test. It includes both the loaded (RLED on) and unloaded (RLED Off) tests. The boost component of the loaded test represents the cost of charging the boost capacitor to the higher voltage level. This has a fixed cost for every loaded check, because the capacitor is gradually discharged during subsequent operations, and the energy is generally not recovered. The other calculations are similar to those shown in Equation 6-1. The unloaded test has a minimal contribution because it involves only some internal reference and comparator circuitry.

6.1.4 BATTERY LIFE

When estimating the battery life, several additional factors must be considered. These include battery resistance, battery self discharge rate, capacitor leakages and the effect of the operating temperature on all of these characteristics. Some number of false alarms and user tests should also be included in any calculation.

For ten year applications, a 3V spiral wound lithium manganese dioxide battery with a laser seal is recommended. These can be found with capacities of 1400 to 1600 mAh.

6.1.5 Functional Timing Diagrams

Figure 6-1 BL5980 Timing Diagram – Standby, No Alarm, Low Supply Test Failure and Chamber Test Failure.

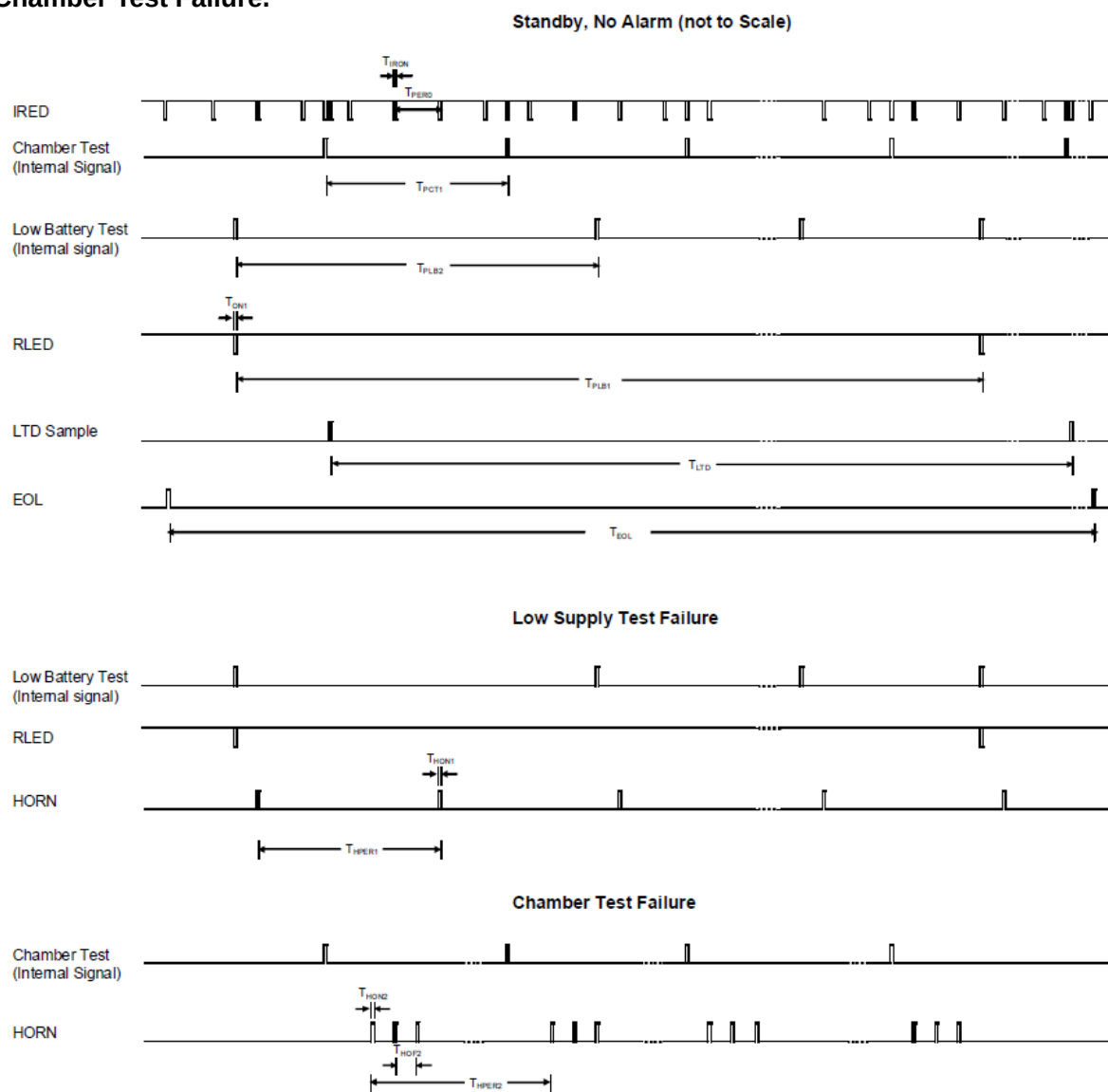


Figure 6-2: BL5980 Timing Diagram – Local

Alarm with Temporal Horn Pattern, Local Alarm with International Horn Pattern, Interconnect as Input with Temporal Horn Pattern and Interconnect as Input with International Horn Pattern.

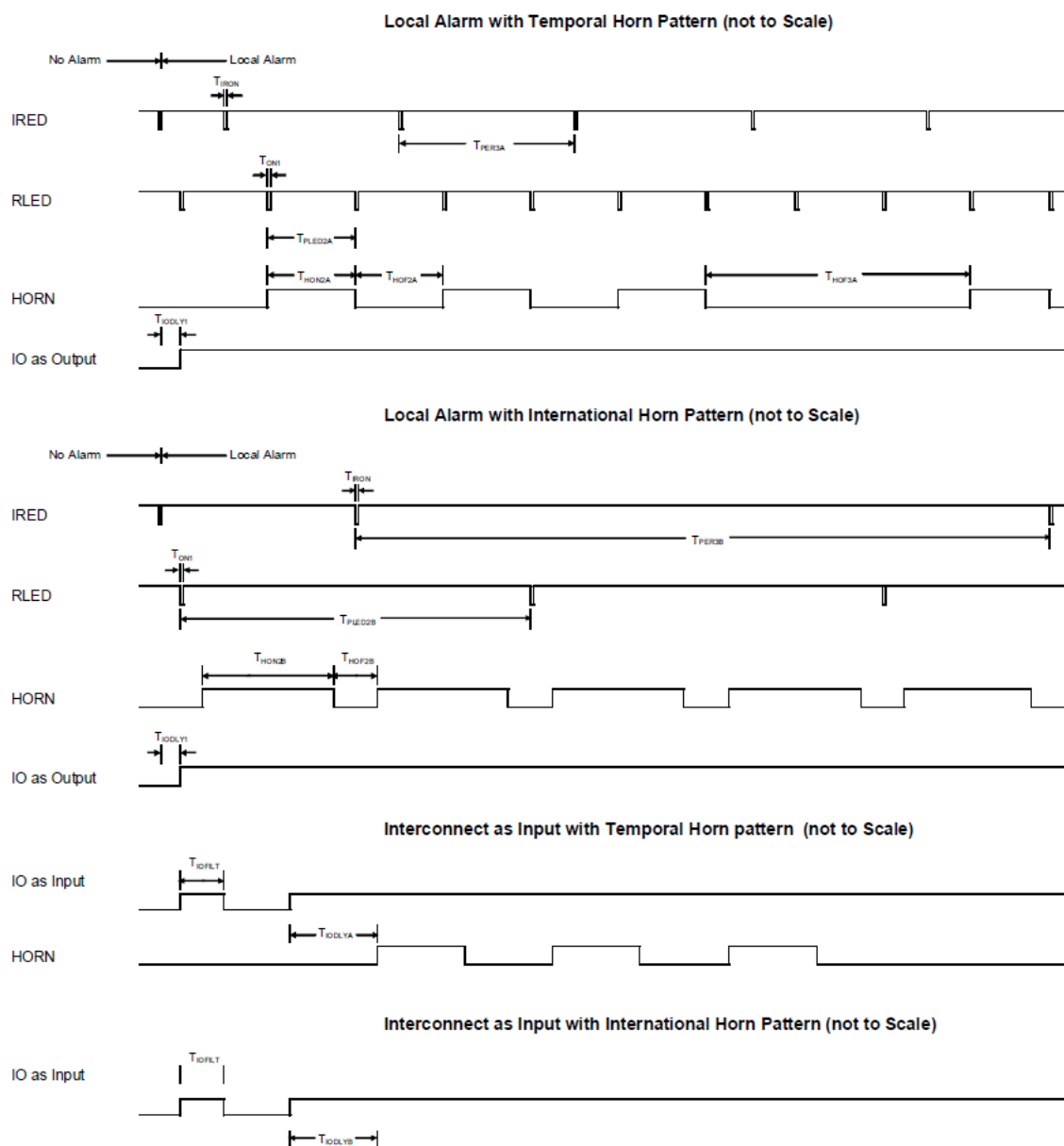
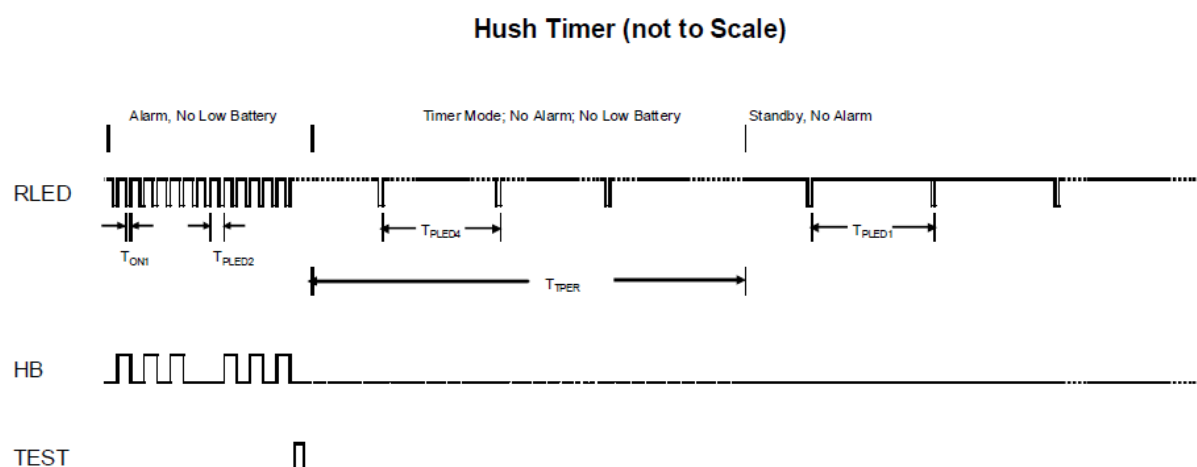
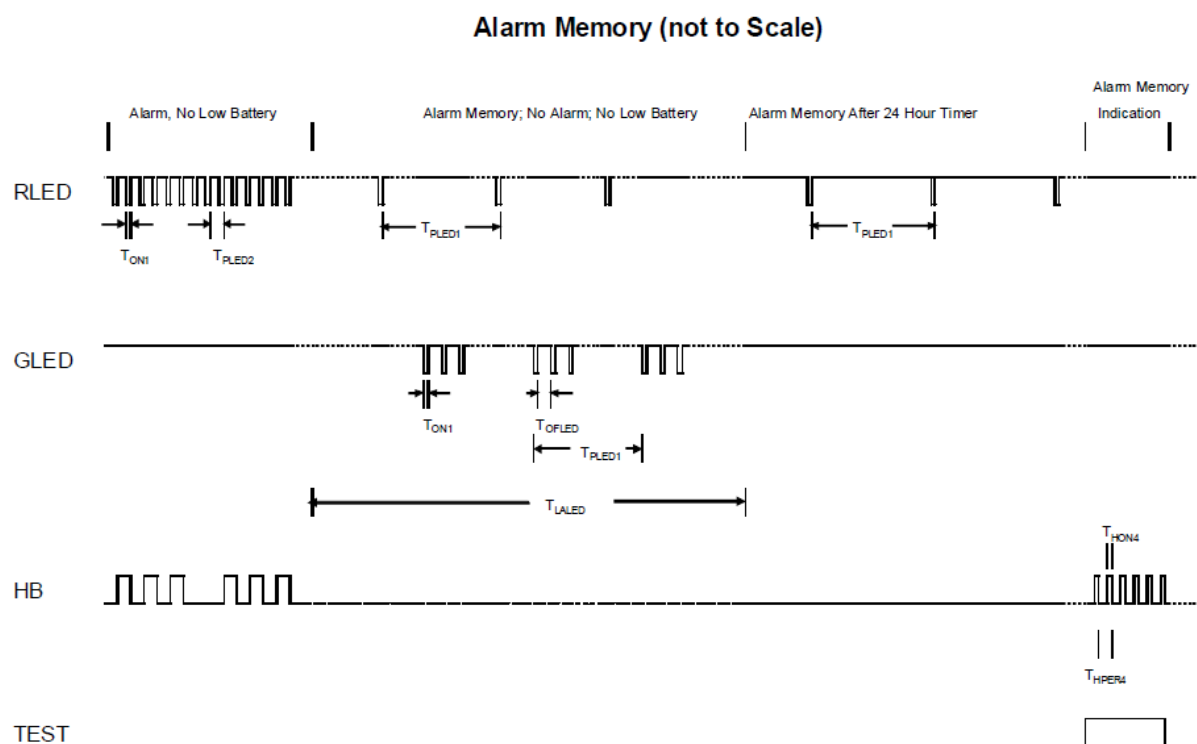


Figure 6-3: BL5980 Timing Diagram – Alarm Memory and Hush Timer.



7.0. PACKAGING INFORMATION

